Standard Dimensions and Tolerances Illustration

Design Guideline Dimensions and Tolerances

CIRCUIT EDGE

0.002" (50.8µm) Minimum Metal to Edge Pullback Spacing Preferred

Resistor Minimum Length and Width
Min 0.001" (25.4µm), Typical 0.002" (50.8µm)

0.002" (50.8µm) Minimum Distance To Circuit Edge Spacing Preferred

0.001" (25.4µm) Minimum Notch Indent per Side of Resistor to Metal Edge

0.006" (152.4µm) Cutout Radius typical

Dicing through metal will typically cause burrs/tails but may be acceptable by the customer’s design

Minimum Notch Via Edge Wrap 0.003" (76.2µm)

Via-Metalized Half Via Edgewrap

Edge Wrap 0.050" (1270µm) minimum

2.5 Mil (63.5µm) minimum

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Top View

Via Hole Diameter Tolerance and Placement
Typical: ±0.002" (50.8µm)
Select: ±0.001" (25.4µm)

One Diameter Spacing Minimum Between Via Holes

0.0025" (63.5µm) Min. Distance From Edge of Conductor Pad to a Via Hole’s Edge (Annular Ring)

One Diameter Spacing Minimum Between Via Holes and Circuit Edge

Side View

Via Hole dia. aspect ratio:
Typical: ≥ 0.80
Select: > 0.50

Aspect ratio is defined as:
\[ \frac{D_v}{T_s} \]

Dv = Diameter of Via Hole
Ts = Thickness of substrate

Resistor Squares compensated for Laser Trim is 0.002" (50.8µm) minimum

Trim Link Area

Serpentine Area

0.0004" (10.16µm) minimum line width

0.0004" (10.16µm) minimum space (gap)

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